In the Specification

Page 8, line 1 amend to read as follows:

(abbreviated as ~~1 x 10E20/cm3~~ $1 \times 10^{20} / cm^{-3}$) and an energy in the range of 1 to 3 kilovolts (kev)

Page 9, line 2 amend to read as follows:

formation of the transistors T1, T2 shown in Fig. 2.

In the Claims

Amend claims 17 and 18 as follows:

17. (Currently Amended) A method of forming a memory cell, comprising:

forming rails of semiconductor material on a substrate;

doping a first portion of said rails;

forming a dielectric on said first portion of at least every other one of said rails;

forming a plate electrode on said first portion of adjacent pairs of said rails;

forming an FET in horizontally along a second portion of said rails adjacent to said first portion which contain the FET source and drain, said FET having a gate electrode disposed on all exposed sides of a part of said second portion of said rails.

18. (Currently Amended) The method of claim 17, wherein said substrate comprises a SOI substrate having a buried insulator layer, and wherein said ~~plurality of~~ rails are disposed on and contact said buried insulator layer.

19. (Original) The method of claim 17, wherein dielectic is formed on said first portions of all of said rails on which a memory cell is to be formed.

20. (Original) The method of claim 19, wherein said rails have a height of at least approximately 0.15 microns.